

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 3 and 25 without prejudice.

- 1 1. (Currently Amended) A computer system comprising:
2 a bus; and
3 a chipset, coupled to the bus, having:
4 an input/output (I/O) buffer, coupled to the bus, to transmit an output
5 signal from the chipset via the bus;
6 a slew rate detection mechanism, coupled to the bus, to detect a slew rate
7 of a the output signal transmitted from the I/O buffer ~~chipset over the bus~~ and to
8 generate a signal indicating a status of the slew rate; and
9 control logic, coupled to the slew rate detection mechanism, to receive the
10 signal and to adjust the slew rate based upon the state of the signal.
- 1 2. (Cancelled)
- 1 3. (Cancelled)
- 1 4. (Previously Presented) The computer system of claim 1 wherein the control
2 logic reduces the slew rate if the signal received from the slew rate detection mechanism
3 indicates that the slew rate is too fast.
- 1 5. (Previously Presented) The computer system of claim 1 wherein the control
2 logic increases the slew rate if the signal received from the slew rate detection
3 mechanism indicates that the slew rate is too slow.

1 6. (Previously Presented) The computer system of claim 1 wherein the slew
2 rate detection mechanism includes a capacitor, coupled to the bus, to integrate the
3 received signal current.

1 7. (Original) The computer system of claim 6 wherein the slew rate detection
2 mechanism further includes:

3 a reference current generator to generate a reference current; and

4 a comparator to compare the received signal current to the reference current.

1 8. (Original) The computer system of claim 7 wherein the slew rate detection
2 mechanism further includes:

3 a first converter, coupled to the capacitor and the comparator to convert the signal
4 current to a signal voltage; and

5 a second converter, coupled to the reference current generator and the comparator
6 to convert the reference to a reference voltage.

1 9. (Original) The computer system of claim 6 wherein the comparator is an
2 operational amplifier.

1 10. (Original) The computer system of claim 1 wherein the bus is a high-speed
2 bus.

1 11. (Currently Amended) A computer system comprising:
2 a main memory device;

3 a memory bus coupled to the main memory device; and
a memory controller, coupled to the bus, having:
4 an input/output (I/O) buffer, coupled to the bus, to transmit an output
5 signal from the memory controller via the bus;
6 a slew rate detection mechanism, coupled to the bus, to detect a slew rate
7 of a the output signal transmitted from the I/O buffer ~~memory controller over the~~
8 ~~bus~~ and to generate a signal indicating a status of the slew rate; and
9 control logic, coupled to the slew rate detection mechanism, to receive the
10 signal and to adjust the slew rate based upon the state of the signal.

1 12. (Cancelled)

1 13. (Previously Presented) The computer system of claim 11 wherein the
2 control logic reduces the slew rate if the signal received from the slew rate detection
3 mechanism indicates that the slew rate is too fast.

1 14. (Previously Presented) The computer system of claim 11 wherein the
2 control logic increases the slew rate if the signal received from the slew rate detection
3 mechanism indicates that the slew rate is too slow.

1 15. (Previously Presented) The computer system of claim 11 wherein the slew
2 rate detection mechanism includes a capacitor, coupled to the bus, to integrate the
3 received signal current.

1 16. (Original) The computer system of claim 15 wherein the slew rate detection
2 mechanism further includes:

3 a reference current generator to generate a reference current; and

4 a comparator to compare the received signal current to the reference current.

1 17. (Original) The computer system of claim 16 wherein the slew rate detection
2 mechanism further includes:

3 a first converter, coupled to the capacitor and the comparator to convert the signal
4 current to a signal voltage; and

5 a second converter, coupled to the reference current generator and the comparator
6 to convert the reference to a reference voltage.

1 18. (Original) A method comprising:

2 transmitting a signal from an input/output (I/O) buffer within a chipset over a bus;

3 receiving the signal at a slew rate detection mechanism within the chipset via the
4 bus;

5 generating a signal indicating the status of the slew rate; and

adjusting the slew rate at control logic within the chipset based upon the signal.

1 19. (Original) The method of claim 18 further comprising generating a reference
2 current at the chipset.

1 20. (Original) The method of claim 19 further comprising:

converting the signal current to a signal voltage;

converting the reference current to a reference voltage; and

comparing the reference voltage to the signal voltage.

21. (Original) The method of claim 18 wherein adjusting the slew rate comprises modifying the amplification of a second signal at the I/O buffer.

22. (Currently Amended) An apparatus comprising:

an input/output (I/O) buffer to transmit an output signal; and

a slew rate detection mechanism coupled to receive the output signal from the I/O buffer via a bus, to detect the slew rate of a the output signal transmitted from the I/O buffer ~~a memory controller~~ over a bus and to generate a signal to indicate the status of the slew rate.

1 23. (Cancelled)

1 24. (Currently Amended) The computer system of claim 22 further comprising
2 control logic, coupled to the I/O buffer and the slew rate detection mechanism, to receive
3 the signal and modify the slew rate based upon the signal.

1 25. (Cancelled)

1 26. (Original) The apparatus of claim 22 wherein the slew rate detection
2 mechanism includes a capacitor, coupled to the bus, to integrate the received signal
3 current.

1 27. (Original) The apparatus of claim 26 wherein the slew rate detection
2 mechanism further includes:
3 a reference current generator to generate a reference current; and
4 a comparator to compare the received signal current to the reference current.

1 28. (Original) The apparatus of claim 27 wherein the slew rate detection
2 mechanism further includes:
3 a first converter, coupled to the capacitor and the comparator to convert the signal
4 current to a signal voltage; and
5 a second converter, coupled to the reference current generator and the comparator
6 to convert the reference to a reference voltage.